**priority under 35 U.S.C. 119 has not be n made in this application.**

## Drawings

Applicant acknowledges receipt of the Notice of Draftsperson's Patent Drawing Review form PTO-948 and that the drawings have been objected to the U.S. Patent Office Draftsperson. Corrected formal drawings including acceptable margins and lines, and characters of uniformly thick and well definition, will be prepared and filed in due course upon indication of allowance of the present application.

## Information Disclosure Material

As requested, a copy of the document "Semiconductor World", as cited in the Information Disclosure Statement filed along with the present divisional application, is enclosed herewith for the Examiner's consideration. Since this application is a divisional application of parent application U.S. Serial No. 09/342,751, and since the above noted document has been made of record in the parent application, a copy of this document was not required in connection with the above noted Information Disclosure Statement. Thus, submission of this document at this time is for the benefit of the Examiner, and payment of corresponding U.S. Patent Office filing fees in connection with submission of this document should not be required.

Also, an Information Disclosure Statement was filed in connection with this application on October 20, 2000, for the purpose of submitting a document cited of

record by the U.S. Patent Office in the above noted parent application U.S. Serial No. 09/342,751. The Examiner is respectively requested to acknowledge receipt of the Information Disclosure Statement and to consider and cite the corresponding document of record in the present application.

**Claim Rejections-35 U.S.C. 103**

Claims 1-4 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art. This rejection is respectfully traversed in view of the following.

As described with respect to prior art Figs. 1A-1C on page 7 of the present application, after the first Rapid Thermal Annealing (RTA) process, **the remaining metal (Co) and (TiN) are selectively removed by a wet process** using ammonia water or a hydrogen peroxide solution, for example. Thereafter, the second RTA process is carried out so that **silicon in SOI layer 18 and in poly-silicon gate layer 22** again react with silicide regions 30 and 32. The silicide regions 30 and 32 thus become $CoSi_2$, which has lower resistance.

However, if SOI layer 18 of the prior art device is formed to have irregular thickness, thinner parts of SOI layer 18 may be silicided entirely. This is because silicon from SOI layer 18 is used to form the silicide region. If the thinner parts of SOI layer 18 are silicided in their entirety, voids may be formed in SOI layer 18. In extreme instances, buried oxide layer (BOX) 14 may be etched when contact holes are formed

in the active area, and silicon substrate 12 may also be etched.

In order to overcome these problems of the conventional fabrication processes, poly-silicon layer 136 is formed over the entire structure in a preferred embodiment of the invention, as illustrated in Fig. 2D. Formation of supplemental poly-silicon layer 136 is performed prior to the second RTA process. As may be readily understood in view of Figs. 2B-2D, supplemental poly-silicon layer 136 is formed **subsequent to removal of Co layer 126 and TiN layer 128,** and after the first RTA process. Because of formation of supplemental poly-silicon layer 136, silicon for the silicide process during the second RTA process is provided not only from SOI layer 118 and poly-silicon gate layer 122, **but also from supplemental silicon layer 136**. Accordingly, the first-reacted silicide regions 130 and 132 respectively formed in SOI layer 118 and in poly-silicon gate layer 122, are converted respectively into second-reacted silicide regions 138 and 140 having lower resistance, as illustrated in Fig. 2E. Because of supplemental poly-silicon layer 136, enough silicon remains in SOI layer 118 after the second RTA process to avoid formation of voids, so that BOX layer 114 is prevented from being etched.

The method for fabricating a semiconductor device using a salicide process of claim 1 includes in combination "performing a first RTA (Rapid Thermal Annealing) process to form a first-reacted silicide region"; "providing a supplemental silicon layer over the surface of the semiconductor device, including the first-reacted silicide region" and "performing a second RTA process to convert the first-reacted silicide region into a second-reacted silicide region, by reaction of the supplemental silicon layer with the first

silicide region". Applicant respectfully submits that prior art Figs. 1A-1C of the present application do not suggest or make obvious these features.

As may be readily understood in view of the description with respect to prior art Figs. 1A-1C as emphasized previously, the supplemental silicon layer of claim 1 provides **an additional source of silicon for the silicide process** carried out during the second RTA process. In conventional fabrication processes as in prior art Figs.1A-1C of the present application for example, only SOI layer 18 and poly-silicon gate layer 22 provide silicon for the second RTA process. By use of the supplemental silicon layer as in the present invention, of the SOI layer is prevented from being entirely depleted during a second RTA process, so that formation of voids therein may be avoided.

The Examiner has suggested that removal of metal layers such as 26 and 28 as described on page 2, lines 13-15 and as illustrated in prior art Figs. 1A-1C of the present application, is performed to "expose silicon which is then silicided by a second RTA **in order to ensure incomplete silicide are not present after the first RTA**...." (our emphasis added). However, as described on page 2, line 16-18, the metal layers are removed and the second RTA process is carried out **so that silicon in the SOI layer and the poly-silicon gate layer again react with the silicide regions.**

Thus, the removal of the metal does not expose silicon that is used as a supplemental silicon layer. On the contrary, removal of the metal exposes the first-reacted silicide regions, so that a second RTA process without the metal layers may be performed. During this second RTA process, the SOI layer and the poly-silicon gate

layer **again function as the only sourc of silicon**. A supplemental silicon layer that serves as an additional source of silicon is not disclosed or even remotely suggested in connection with prior art Figs. 1A-1C of the present application. As a result, the SOI layer is further depleted of silicon, creating voids therein.

Applicant thus respectfully submits that the description of prior art Figs. 1A-1C of the present application does not disclose or even remotely suggest a supplemental silicon layer. The prior art as relied upon by the Examiner fails to suggest or make obvious a method for fabricating a semiconductor device including in combination "performing a second RTA process to convert the first-reacted silicide region into a second-reacted silicide region, by reaction of the supplemental silicon layer with the first-reacted silicide region", as in claim 1. In absence of a prior art reference of teaching specifically disclosing a supplemental silicon layer used in connection with a second RTA process as a silicon source, the Examiner has relied upon impermissible hindsight to maintain this rejection. Applicant therefore respectfully submits that the method for fabricating a semiconductor device of claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner, and that this rejection of claims 1-4 is improper for at least these reasons.

Claims 5-9 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art, and in view of the Burgener reference (U.S. Patent No. 5,863,823). This rejection is respectfully traversed in view of the following.

The Examiner has acknowledged that Applicant's admitted prior art does not

specifically teach a supplemental silicon layer that is amorphous and that is formed by sputtering. As emphasized above, the description of prior art Figs. 1A-1C of the present application do not disclose or suggest a supplemental poly-silicon layer. Applicant respectfully submits that the Burgener reference as relied upon by the Examiner also fails to provide the necessary motivation to use a supplemental poly-silicon layer as in the present invention, and more particularly an amorphous supplemental silicon layer.

Specifically, the Burgener reference describes in column 5, lines 19-35 thermal annealing of amorphous region 22A illustrated in Figs. 1A-1C. However, the thermal annealing induces solid phase epitaxial regrowth from the surface of monocrystalline silicon region 22S, downward through amorphous region 22A to interface 18. Amorphous region 22A is thus regrown as single crystal region 26. Thereafter, further annealing is performed to remove remaining defects or states, thus converting amorphous region 22A into a substantially pure silicon crystal region devoid of twins and band gap states 14 and 16, respectively.

Accordingly, amorphous silicon layer 22A of the Burgener reference is not formed prior to a second RTA process, and does not convert a first-reacted silicide region into a second-reacted silicide region, by reaction with a first-reacted silicide region. The Burgener reference as relied upon by the Examiner thus fails to overcome the above noted deficiencies of prior art Figs. 1A-1C of the present application. Applicant therefore respectfully submits that the method for fabricating a semiconductor device of claims 5-9 would not have been obvious in view of the prior art as relied upon

by the Examiner taken singularly or together, and that this rejection is improper for at least these reasons.

**Claims 19-22**

Applicant respectfully submits that claims 19-22, as dependent respectively on claims 1 and 9, distinguish over and would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, for at least the above reasons and in further view of the features therein.

**Conclusion**

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections and to pass all the claims of the present application to issue for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of one (1 ) month to November 18, 2000 for the period in which to file a response to the outstanding Office Action. The required fee is attached hereto.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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AJT:cej

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Enclosures: Copy of "Semiconductor World" document